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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/587,465	06/05/2000	Jung-Cheng Lin	TSMC99-700	7855

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EXAMINER
SARKAR, ASOK K

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/587,465	LIN, JUNG-CHENG	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim R jections - 35 USC § 103

1. Claims 1 - 26 rejected under 35 U. S.C. 103(a) as being unpatentable for reasons of record in Paper No. 5 is reproduced below:

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1 – 10, 12 – 23, 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein, US 6,181,012 in view of Danek, US 5,943799 and Hsu, US 6,194,310, US 6,194,310.

Regarding claims 1 and 14, Edelstein teaches a method to prevent copper Diffusion in an integrated circuit comprising:

- providing a substrate of wafer 52 (column 6, line 1) having an insulator layer 54 (column 6, line 62) deposited on the substrate 52 with reference to Fig. 2;
- providing first level of conducting wire 46 (column 6, line 64) over the insulator layer with reference to Fig. 2;
- depositing first and second dielectric layer 54 (column 6, line 62) over the first level of conducting wire 46 with reference to Fig. 2;
- patterning and etching the dielectric layers forming dual damascene trench/via openings 84 (column 7, line 40) with reference to Figs. 2 and 4A;
- depositing a barrier layer 72 (column 7, line 39) of W, WN and WSiN (column 9, line 31) with reference to Figs. 2 and 4A;

- depositing by electrochemical deposition (ECD) (column 7, line 57) a copper seed layer 76 or 86 (column 9, line 35);
- depositing by ECD copper conducting material 90 (column 7, line 42) over the seed layer (see column 7, lines 57 – 61) with reference to Figs. 2 and 4C and removing excess material layers to form the copper dual inlaid structure (see Figs. 2 and 4C) in column 7, lines 43 - 46;

Edelstein teaches barriers containing materials such as W, WN and WSiN but fails to expressly teach depositing a first barrier layer of WN, then silanize the WN layer with silane gas to form WSiN over WN and depositing a W barrier layer to form a composite diffusion barrier layer structure of W / WSiN / WN.

Danek teaches a method of depositing composite multi-layer barrier structures especially comprising a layer sequence of W / WSiN / WN with reference to Figs 1 and 2 throughout the disclosure. Danek teaches the desirability of designing a suitable multi-layered diffusion layers in terms of integrity, resistivity and adhesion among other things in great detail. Danek teaches that TiSiN can be made by silane treatment of TiN and Hsu teaches that the same process can be applied for WSiN in column 5, lines 20 –24.

Danek and Hsu fail to expressly teach the processing steps of providing insulator/dielectric layers, patterning and etching to form trench to be filled by Cu seed layer and ECD Cu layer.

However, given the substantial teaching of Edelstein in view of Danek and Hsu, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure by incorporating multi-

layer barrier structure taught by Danek and Hsu by depositing a first barrier layer of WN, then silanize the WN layer with silane gas to form WSiN over WN and depositing a W barrier layer to form a composite diffusion barrier layer structure of W / WSiN / WN so that a greatly improved barrier layer is formed to prevent Cu diffusion.

Regarding claims 2 and 15, Edelstein teaches substrate 52 as an IC module with CMOS devices in column 6, lines 51 – 61.

Regarding claims 3 and 16, Edelstein teaches silicon dioxide dielectric/insulator in column 2, line 9.

Regarding claims 4 - 7 and 17 - 20, Edelstein does not expressly teach the deposition process or the thickness of the WN barrier layer.

Danek teaches W and WN deposition by CVD and PECVD in column 5, lines 14 – 18 and barrier thickness less than 100 Angstroms in column 2, line31.

Therefore, given the substantial teaching of Edelstein in view of Danek and Hsu, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to have the composite layered structure with appropriate thickness through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen

methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Regarding claims 8 and 21, Edelstein fails to expressly teach the method of forming the WSiN layer.

Danek teaches the method for forming TiSiN by the silane treatment with ammonia at a temperature of 300°C in column 5, line 60 and column 6, line 14. As described earlier, Hsu teaches that processing of WSiN is similar to Ti.

Therefore, given the substantial teaching of Edelstein in view of Danek and Hsu, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to have the composite layered structure containing WSiN layer on WN layer of appropriate thickness through routine experimentation and optimization to achieve optimum benefits.

Regarding claims 9 and 22, Edelstein teaches seed layer formation by ECD, PVD and thickness in column 9, lines 31 – 45.

Regarding claims 10 and 23, Edelstein teaches ECD process for forming the main copper conductor in column 7, lines 57 – 60.

Regarding claims 12 and 25, Edelstein teaches planarization to remove excess Cu by CMP in column 7, lines 44 – 46.

Regarding claims 13 and 26, Edelstein teaches multilevel interconnect structures for VLSI under the heading background of the invention.

Edelstein in view of Danek and Hsu does not expressly teach creating multilevel structure by repeating the processes of claim 1 and 14.

However, given the substantial teaching of Edelstein in view of Danek and Hsu, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to create multilevel structure by repeating the processes of claim 1 and 14.

4. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein, US 6,181,012 in view of Danek, US 5,943799 and Hsu, US 6,194,310, US 6,194,310 as applied to claims 1 and 14 above, and further in view of Yu, US 6,291,332 and Hsu, US 6,054,382.

5. Edelstein in view of Danek and Hsu fails to teach ECD copper deposited on seed layer and barrier layer with fine grained <111> structure.

Yu teaches the relevance of <11> seed deposition which will ultimately result in

fine grained Cu plug of <111> orientation in column 2, lines 28 – 40.

Hsu teaches the desirability of <111> texture of metal conductors for electromigration resistance in column 1, lines 21 – 26.

Therefore, given the substantial teaching of Edelstein in view of Danek and Hsu, and further in view of Yu and Hsu, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's ECD Cu deposition in the trench so that fine grained Cu plug of <111> orientation is formed. <111> Cu texture results in the growth of fine-grained structure and fine-

grained <111> textured Cu structure is more resistant to electromigration than the face-centered cube texture <100>.

6. Claims 1 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein, US 6,181,012 in view of Koyama, US 5,990,008.

These claims combined with other prior arts as were described in the Previous paragraphs can also be rejected as being unpatentable over Edelstein in view of Koyama.

Koyama teaches dual layer barrier structure of WN and WSiN in column 7, lines 4 – 17.

Response to Arguments

7. Applicant's arguments filed May 28, 2002 have been fully considered but they are not persuasive.

8. Applicant contends that the present invention is directed towards a process of forming an improved copper metal diffusion barrier layer having a structure: W / WSiN / WN. The structure is formed by depositing WN at the bottom, then forming WSiN by in-situ silanization and then by final deposition of W.

9. In response to Applicant's arguments that Danek's invention does not contain any claim to diffusion barrier compounds, elements, layers or material, the Applicant is directed to the title of the disclosure and the whole disclosure is about forming various kinds of barrier materials in multiplayer forms as is shown in Figs 1, 2, 4 and 6 of their disclosure including the three layer barrier structure W / WSiN / WN.

10. In the same manner, Koyama teaches a dual barrier layer constructed of materials chosen from a group in column 7, lines 11 – 12.

11. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the multilayer barrier structures taught by Danek covers the barrier structure of the instant Application. Silanization of metal nitride layers are also well known by the prior art as was used in rejecting the claims.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Sherry can be reached on 703 308 1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar
June 19, 2002

6/24/02

MICHAEL SHERRY
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TECHNOLOGY CENTER 2800